1. A method to form a floating gate for a memory device, said method comprising:

forming a first conductor layer overlying a substrate with a gate dielectric layer therebetween;

forming a masking layer overlying said first conductor layer;

patterning said masking layer to expose first regions of and to cover second regions of said first conductor layer;

forming a plurality of first concave surfaces on said first regions of said first conductor layer;

removing said masking layer;

forming a plurality of second concave surfaces on said second regions of said first conductor layer; and

patterning said first conductor layer to form floating gates wherein the interfaces between said plurality of first and second concave surfaces form vertical tips on said floating gates.

2. The method according to Claim 1 wherein said step of forming a plurality of first concave surfaces on said first conductor layer first regions comprises converting part of said first conductor layer into a first oxide layer.

3. The method according to Claim 2 wherein said first oxide layer is removed prior to said step of depositing a second dielectric layer overlying said first conductor layer.

4. The method according to Claim 2 wherein said converting comprises thermal oxidation of said first conductor layer.

5. The method according to Claim 1 wherein said step of forming a plurality of second concave surfaces on said first conductor layer second regions comprises converting part of said first conductor layer into a second oxide layer.

6. The method according to Claim 5 wherein said second oxide layer is removed prior to said step of depositing a second dielectric layer overlying said first conductor layer.

7. The method according to Claim 5 wherein said converting comprises thermal oxidation of said first conductor layer.

8. The method according to Claim 1 wherein said first conductor layer comprises polysilicon.

9. The method according to Claim 1 and further comprising the steps of:

depositing a second dielectric layer overlying said first conductor layer prior to said step of patterning said first conductor layer;

depositing a second conductor layer overlying said second dielectric layer; and

patterning said second conductor layer and said second dielectric layer to form control gates wherein said control gates overlie said floating gates.

10. The method according to Claim 9 and further comprising the step of implanting ions into said substrate to form source and drain regions for said flash memory devices.

11. A method to form a floating gate for a flash memory device, said method comprising:

forming a first conductor layer overlying a substrate with a gate dielectric layer therebetween;

depositing a masking layer overlying said first conductor layer;

patterning said masking layer to expose first regions of and to cover second regions of said first conductor layer;

forming a plurality of first concave surfaces on said first conductor layer first regions by converting part of said first conductor layer into a first oxide layer;

removing said masking layer;

forming a plurality of second concave surfaces on said first conductor layer second regions by converting part of said first conductor layer into a second oxide layer;

removing said first and second oxide layers; and

patterning said first conductor layer to form floating gates wherein the interfaces between said plurality of first and second concave surfaces form vertical tips on said floating gates.

12. The method according to Claim 11 wherein said steps of converting said first conductor layer into first and second oxide layers comprise thermal oxidation of said first conductor layer.

13. The method according to Claim 11 wherein said first conductor layer comprises polysilicon.

14. The method according to Claim 11 and further comprising the steps of:

depositing a second dielectric layer overlying said first conductor layer prior to said step of patterning said first conductor layer;

depositing a second conductor layer overlying said second dielectric layer; and

patterning said second conductor layer and said second dielectric layer to form control gates wherein said control gates overlie said floating gates.

15. The method according to Claim 14 and further comprising the step of implanting ions into said substrate to form source and drain regions for said flash memory devices.

16. A flash memory device comprising:

a substrate;

a floating gate overlying said substrate wherein said floating gate comprises:

a gate dielectric layer overlying said substrate; and

a first conductor layer overlying said gate dielectric layer wherein said first conductor layer comprises first and second concave surfaces and

wherein the interfaces between said first and second concave surfaces form vertical tips on said floating gate; and

a control gate overlying said floating gate wherein said control gate comprises:

a second dielectric layer overlying said floating gate; and

a second conductor layer overlying said second dielectric layer.

17. The device according to Claim 16 wherein said first conductor layer comprises polysilicon.

18. The device according to Claim 16 wherein said gate dielectric layer comprises silicon oxide.

19. The device according to Claim 16 wherein said second conductor layer comprises polysilicon.

20. The device according to Claim 16 and further comprising source and drain regions in said substrate aligned to said floating gate.

21. A method to form an electron emitter, comprising:

forming a conductor layer on a substrate;

forming a plurality of continuous concave surfaces on said conductor layer; and

patterning said conductor layer to form a plurality of vertical tips between said plurality of continuous concave surfaces on said electron emitter.

22. The method according to Claim 21 wherein said step of forming a plurality of continuous concave surfaces on said conductor layer comprises converting part of said conductor layer into an oxide layer.

23. The method according to Claim 22 wherein said oxide layer is removed prior to said step of patterning said conductor layer.

24. The method according to Claim 22 wherein said converting comprises thermal oxidation of said conductor layer.

25. The method according to Claim 21 wherein said conductor layer comprises polysilicon.

26. An electron emitter device comprising:

a substrate; and

an electron emitter overlying said substrate wherein said electron emitter comprises a conductor layer with a surface having a plurality of vertical tips between a plurality of concave surfaces.

27. The device according to Claim 26 wherein said conductor layer comprises polysilicon.